

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No		09/468,247
Priority Filing Date		12/20/99
Inventor		Perino et al
Applicant		
Priority Group Art Unit		2833
Priority Examiner		Paumer
Attorney's Docket No		RB1-035USC3
Title: Chip Socket Assembly and Chip File	e Assembly for Semiconductor Ch	ips

CONTINUATION PATENT APPLICATION TRANSMITTAL

To:

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Commissioner of Patents and Trademarks,

Washington, D.C. 20231

From:

Daniel L. Hayes (Tel. 509-324-9256; Fax 509-323-8979)

Customer No. 29150



29150

PATENT & TRADEMARK OFFICE

The following enumerated items accompany this transmittal letter and are being submitted for the matter identified in the above caption.

- 1. Transmittal Letter with Certificate of Mailing included.
- 2. Fee Transmittal
- 3. Check in the Amount of \$764.00
- 4. PTO Return Postcard Receipt
- 5. Request for Continuation Application Under 37 C.F.R. 1.53 (b)
- 6. True copy of the prior application as filed including the specification (62 pages, claims 1-67 & Abstract)
- 7. Copy of Executed Declaration
- 8. Preliminary Amendment
- 9. Information Disclosure Statement, including form PTO-1449
- 10. Substitute Drawing Request
- 11. 14 Sheets Substitute Drawings (Figs. 1-38)
- 12. Copy of Assignment

Large Entity Status [x]

Small Entity Status []

The Commissioner is hereby authorized to charge payment of fees or credit overpayments to Deposit Account No. 12-0769 in connection with any patent application processing fees under 37 CFR 1.17; and any additional filing fees under 37 CFR 1.16 for the presentation of extra claims.

Date: 9/20/01

Daniel L. Hayes

Reg. No. 34,618



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No.	09/468,247
Priority Filing Date	12/20/1999
Inventor	Perino et al.
Applicant	Rambus, Inc.
Priority Group Art Unit	2833
Priority Examiner	Paumen
Attornev's Docket No	RB1-035USC3
Title: Chip Socket Assembly and Chip File Assembly for S	emiconductor Chips

REQUEST FOR CONTINUATION APPLICATION

UNDER 37 C.F.R. 1.53(b)

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Commissioner of Patents and Trademarks,

Washington, D.C. 20231

From:

Daniel L. Hayes (Tel. 509-324-9256; Fax 509-323-8979)

Customer No. 29150

29150

PATENT & TRADEMARK OFFICE

This is a request for filing a Continuation application under 37 CFR §1.53(b) of Application Serial No. 09/468,247 which was filed December 20, 1999 and is entitled "Chip Socket Assembly and Chip File Assembly for Semiconductor Chips" The prior application was submitted in the names of Perino et al. The original declaration showing their addresses is also enclosed.

The prior application was a complete application as set forth in 37 CFR §1.51(a). The application papers being filed herewith are a true copy of the prior application as filed including the specification (with claims), drawings, oath or declaration showing the signature(s), and any amendments referred to in the oath or

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declaration to complete the prior application. No amendments referred to in the oath or declaration filed to complete the prior application introduced new matter therein. No abandonment or termination of proceeding has occurred in the above-identified prior application.

The filing date of pending application Serial No. 09/468,247 is hereby claimed under 35 U.S.C. §120.

A preliminary amendment is enclosed.

A check is enclosed to pay fees under 37 CFR §1.16 and §1.17 associated with this communication.

A previous assignment to Rambus, Inc. has been executed by the inventors in the prior application, and is applicable to the present application. A copy of the assignment is enclosed herewith.

A previous power of attorney in the prior application is given to Lewis C. Lee, Reg. No. 34,656, Daniel L. Hayes, Reg. No. 34,618, Allan T. Sponseller, Reg. 38,318; Steven R. Sponseller, Reg. No. 39,384; James R. Banowsky, Reg. No. 37,773; Lance R. Sadler, Reg. No. 38,605; Thomas A. Jolly, Reg. No. 39,241; David A. Morasch, Reg. No. 42,905; Kasey C. Christie, Reg. No. 40,559; Nathan R. Rieth, Reg. No. 44,302; Brian G. Hart, Reg. No. 44,421; David S. Thompson, Reg. No. 37,954; Paul W. Mitchell, Reg. No. 44,453; Bradley K. DeSandro, Reg. No. 34,521; and Brian J. Pangrle, Reg. No. 42,973. A copy of which is enclosed herewith.

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Please send correspondence to: Customer No. 29150.
Direct telephone calls to: Daniel L. Hayes (509) 324-9256.

Respectfully submitted,

Dated: <u>1/20/01</u> By: <u>Dated</u>: A

Daniel L. Hayes Reg. No. 34,618

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PTO/SB/17 (11-00)
Approved for use through 10/31/2002. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Juder the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

FEE TRANSMITTAL for FY 2001

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT

(\$) 764.00

Col	mplete if Kn wn	
Application Number	09/468,247	
Filing Date	12/20/99	
First Named Inventor	Perino et al.	
Examiner Name	Paumen	
Group Art Unit	2833	
Attorney Docket No.	KB1-035U5C3	_

METHOD OF PAYMENT	FEE CALCULATION (continued)	
The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:	3. ADDITIONAL FEES	
indicated fees and credit any overpayments to:	Large Small	
Account 12-07-1.4	Entity Entity Fee	Fee Paid
Number 2 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0	Code (\$) Code (\$)	
Account / P.P. Y HOMES, P. L.	105 130 205 65 Surcharge - late filing fee or oath	
Name Charge Any Additional Fee Required	127 50 227 25 Surcharge - late provisional filing fee or cover sheet	
Under 37 CFR 1.16 and 1.17		
Applicant claims small entity status. See 37 CFR 1.27		
2. Payment Enclosed:		
Check C Credit card Money Other	112 920* 112 920* Requesting publication of SIR prior to Examiner action	
Order —	113 1,840* 113 1,840* Requesting publication of SIR after Examiner action	
FEE CALCULATION	115 110 215 55 Extension for reply within first month	
1. BASIC FILING FEE	116 390 216 195 Extension for reply within second month	
Large Entity Small Entity Fee Fee Fee Fee Description	117 890 217 445 Extension for reply within third month	
Code (\$) Code (\$) Fee Paid	118 1,390 218 695 Extension for reply within fourth month	
101 710 201 355 Utility filing fee	128 1,890 228 945 Extension for reply within fifth month	
106 320 206 160 .Design filing fee	119 310 219 155 Notice of Appeal	<u> </u>
107 490 207 245 Plant filing fee	120 310 220 155 Filing a brief in support of an appeal	
108 710 208 355 Reissue filing fee	121 270 221 135 Request for oral hearing	
114 150 214 75 Provisional filing fee	138 1,510 138 1,510 Petition to institute a public use proceeding	
SUBTOTAL (1) (\$) 710	140 110 240 55 Petition to revive - unavoidable	
2. EXTRA CLAIM FEES	141 1,240 241 620 Petition to revive - unintentional	
Fee from Extra Claims <u>below</u> <u>Fee Paid</u>	142 1,240 242 620 Utility issue fee (or reissue)	
Total Claims 23 -20** = 3 × 78 = 54	143 440 243 220 Design issue fee	
Independent 2 - 3** = X X = 3	144 600 244 300 Plant issue fee	
Multiple Dependent =	122 130 122 130 Petitions to the Commissioner	
	. 123 50 123 50 Processing fee under 37 CFR 1.17(q)	
Large Entity Small Entity Fee Fee Fee Fee Fee Description	126 180 126 180 Submission of Information Disclosure Stmt	
Fee Fee Fee Fee Fee Description Code (\$) Code (\$) 103 18 203 9 Claims in excess of 20	581 40 581 40 Recording each patent assignment per property (times number of properties)	*
102 80 202 40 Independent claims in excess of 3	146 710 246 355 Filing a submission after final rejection (37 CFR § 1.129(a))	-
104 270 204 135 Multiple dependent claim, if not paid	149 710 249 355 For each additional invention to be	
109 80 209 40 ** Reissue independent claims over original patent	examined (37 CFR § 1.129(b))	
110 18 210 9 ** Reissue claims in excess of 20	179 710 279 355 Request for Continued Examination (RCE)	
and over original patent	169 900 169 900 Request for expedited examination of a design application	
SUBTOTAL (2) (\$) 54	Other fee (specify)	<u> </u>
**or number previously paid, if greater; For Reissues, see above	*Reduced by Basic Filing Fee Paid SUBTOTAL (3) (\$)	

SUBMITTED BY			Complete (if applicable)
Name (PrintlType)	Daniel L. Haves	Registration No. 34, 418	Telephone (509) 324-9256
Signature	1 Janis / Atanos		Date 9/20/0/

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

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Title: Chip Socket Assembly and Chip File Assem	ably for Semiconductor Chips

SUBSTITUTE DRAWING REQUEST

To:

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Drawing Review Branch

Commissioner of Patents and Trademarks,

Washington, D.C. 20231

From:

Daniel L. Hayes (Tel. 509-324-9256; Fax 509-323-8979)

Customer No. 29150



TATELIT & TOADEMARY OFFIC

Applicant submits herewith a new set of formal drawings to correct informalities noted by the official draftsperson in Priority Application.

Respectfully Submitted,

Date: 9/20/01

By:

Daniel L. Hayes Reg. No. 34,618 (509) 324-9256

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CERTIFICATE OF MAILING

I hereby certify that the items listed above as enclosed are being deposited with the U.S. Postal Service as either first class mail, or Express Mail if the blank for Express Mail No. is completed below, in an envelope addressed to The Commissioner of Patents and Trademarks, Washington, D.C. 20231, on the below-indicated date. Any Express Mail No. has also been marked on the listed items.

Express Mail No. (if applicable) ___ Date: